Embodiment 3

FIGS. 3A through 3F illustrate a novel method for fabricating a MOSFET according to a third embodiment of the present invention.

Referring to FIG. 3A, a gate insulating layer **32** of, for example, an oxide and a polysilicon gate **33** are sequentially formed on an active region or an n type well of a semiconductor substrate **31**, and are patterned by a photolithography and an etching process. As a result, a gate pattern consisting of the gate oxide layer **32** and the polysilicon gate **33** is formed. Next, a phosphorous (or boron) ion implantation into the semiconductor substrate **31** is carried out using the gate pattern as a mask to form an n^- type (or p^- type) impurity region **34** of low concentration on both sides of the gate pattern.

With reference to FIGS. 3B and 3C, a first insulating layer **35** of, for example, SiO_2 or SiN is deposited over the semiconductor substrate **31**, including the gate pattern, and then a second insulating layer **36** of, for example, SiO_2 or SiN is also deposited on the first insulating layer **35**. The first insulating layer **35** has a thickness of about 30 Å or more, and the second insulating layer **36** is formed thicker than the first insulating layer **35**.

As shown in FIG. 3D, an anisotropic etch process of the second insulating layer **36** is carried out until an upper surface of the first insulating layer **35**, to thereby form a sidewall spacer **36***a* on both sidewalls of the gate pattern. As a result, a gate structure is formed which includes the gate oxide layer **32**, the polysilicon gate **33** and the sidewall spacer **36***a*. Next, an arsenic (or BF_2) ion implantation using the gate structure as a mask is carried out to form an n^+ type (or p^+ type) impurity region **37**. As a result, a source/drain **38** is completely formed which has an LDD (lightly doped drain) structure consisting of the low concentration impurity region (lightly doped source/drain extension) **34** and the high concentration impurity region (source/drain region) **37**. During the ion implantation, the first insulating layer **35** is used as a buffering layer which is capable of preventing the active region of the semiconductor substrate from becoming damaged.

In FIG. 3E, after removal of the first insulating layer **35***b* exposed on both the upper surfaces of the polysilicon gate **33** and the source/drain region **37**, a magnetic transition metal layer **39** is formed having a thickness of 100 Å to 250 Å (preferably, a thickness of about 150 Å) by PVD or CVD using plasma. The transition metal layer **39** may be made of at least one selected from a group consisting of Co, Ti, Ni and the like.

Finally, as shown in FIG. 3F, an annealing is performed so that a self-aligned silicide layer **40** having a thickness of 400 Å to 800 Å can be formed at both tops of the polysilicon gate **33** and the source/drain region **37** by reaction with the transition metal layer **39**. In this embodiment, the annealing is accomplished by two continuous steps, a low-temperature RTA (rapid thermal annealing), preferably at a temperature of 400° to 500°, and a high-temperature thermal annealing of preferably, a temperature of approximately 650° or more, which are identical with the first embodiment.

After formation of the silicide layer **40**, unreacted portions of the transition metal layer **39** are selectively removed, and then metalization is performed as is well-known in the art. As a result, a MOSFET is completely fabricated.

Thus, the present invention has the advantage of using an LDD-forming method, which can protect an active region of a semiconductor substrate from becoming damaged during an ion implantation for forming a source/drain region of high concentration, because of a buffering layer formed on the active region. Therefore, MOSFET devices which are manufactured according to the method can exhibit improved electrical characteristics.

What is claimed is:

1. A method for fabricating a metal oxide semiconductor (MOS) transistor, comprising:

forming a gate pattern on a semiconductor substrate of a first conductivity type, said gate pattern including a gate insulating layer and a polysilicon gate sequentially formed thereon;

injecting low concentration impurity ions of a second conductivity type into the semiconductor substrate, using the gate pattern as a mask, to form lightly doped regions at both sides of the gate pattern;

forming an insulating layer on the semiconductor substrate, including the gate pattern;

anisotropically etching the insulating layer to form sidewall spacers on both sidewalls of the gate pattern and to leave a portion of the insulating layer on the semiconductor substrate, wherein the gate pattern and the sidewall spacers constitute a gate structure;

injecting high concentration impurity ions of the second conductivity type into the semiconductor substrate, using the gate structure as a mask, to form heavily doped regions at both sides of the gate structure;

removing said portion of the insulating layer to expose an upper surface of the heavily doped region, wherein the lightly and heavily doped regions constitute a source/drain;

forming a transition metal layer over the semiconductor substrate, including the gate structure; and

annealing the semiconductor substrate to form a silicide layer on an upper surface of the polysilicon gate and on the heavily doped regions based on reaction of the transition metal layer with the polysilicon gate and the heavily doped regions.

2. A method for fabricating a metal oxide semiconductor (MOS) transistor, comprising:

forming a gate pattern on a semiconductor substrate of a first conductivity type, said gate pattern including a gate insulating layer and a polysilicon gate sequentially formed thereon;

injecting low concentration impurity ions of a second conductivity type into the semiconductor substrate, using the gate pattern as a mask, to form lightly doped regions at both sides of the gate pattern;

forming sidewall spacers on both sidewalls of the gate pattern to form a gate structure consisting of the gate pattern and the spacers;

forming a buffering layer over the semiconductor substrate, including over the gate structure and the lightly doped regions;

with the buffering layer disposed over the lightly doped regions at both sides of the gate structure, injecting high concentration impurity ions of the second conductivity type through the buffering layer into the semiconductor substrate, using the gate structure as a mask, to form heavily doped regions at both sides of the gate structure;

removing the buffering layer to expose an upper surface of the heavily doped regions and the gate structure, wherein the lightly and heavily doped regions constitute a source/drain;

once the buffering layer has been removed, forming a transition metal layer over the semiconductor substrate,

including over the sidewall spacers and polysilicon gate of the exposed gate structure and the exposed heavily doped regions; and

annealing the semiconductor substrate to form a silicide layer on an upper surface of the polysilicon gate and on the heavily doped regions based on reaction of the transition metal layer with the polysilicon gate and the heavily doped regions;

wherein said buffering layer has a thickness sufficient to prevent the lightly doped regions from becoming damaged during said ion injection for forming said heavily doped regions.

3. The method according to claim 2, wherein said transition metal layer is magnetic.

4. The method according to claim 3, wherein said magnetic transition metal layer comprises at least one selected from a group consisting of cobalt, titanium, or nickel.

5. The method according to claim 2, wherein said buffering layer comprises an insulator.

6. The method according to claim 5, wherein said insulator comprises SiO_2 or SiN.

7. The method according to claim 2, wherein said thickness of said buffering layer is about 30 Å.

8. The method according to claim 2, wherein said transition metal layer is formed by physical vapor deposition or chemical vapor deposition using plasma.

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